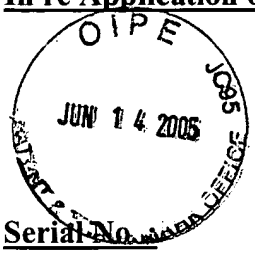
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :



Aritharan Thurairajaratnam
Mohan Nagar
Anand Govind
Farshad Ghahghahi

Serial No. 10/620,057

Filed : July 15, 2003

For : Measurement Of Package Interconnect Impedance Using Tester And Supporting Tester

Group Art Unit : 2829

Examiner : Chan, Emily Y.

Atty Docket : / 02-4456/1P

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

6/14/05 Connie Del Castillo

Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 14 JUN 05